In The Claims

Applicant submits below a complete listing of the current claims, with insertions, if any, indicated by underlining and deletions, if any, indicated by strikeouts and/or double bracketing.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

Please cancel claims 1.-3.

4. (Currently amended) A circuit for regenerating a clock signal based on two complementary signals by means of a D flip-flop, a clock input of which receives the result of a logic combination of two shaping signals resulting from a filtering of the respective rising edges of the complementary signals, wherein a reset input of the flip-flop receives one of said shaping signals,

wherein the logic combination is of NAND type, the shaping signals being provided by inverters, and

wherein the reset input of the flip-flop is connected at the output of one of the inverters for shaping the complementary signal, of which an output of the flip-flop provides an inverted image.

Please cancel claims 5 - 6.

7. (Previously Presented) An interface system between a modem and a transmission line, of the type using a capacitive isolation barrier to transmit a clock for modulating the signals to be transmitted from the modem to a processing circuit on the transmission line side of the interface system, including the clock regeneration circuit of claim 4.

8. (Currently amended) A clock signal regeneration circuit, comprising:

a first input for a clock signal and a second input for an inverted clock signal;

logic to shape the clock signal into a first signal and the inverted clock signal into a second signal;

a flip-flop; [and]